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WHAT IS CLAIMED IS

1. A semiconductor device, comprising:

transfer gates;

contact plugs adjacent to said transfer gates;

said each transfer gate having a gate insulating film, a gate electrode layer, and side walls for covering sides of said gate insulating film and said gate electrode layer;

said each contact plug having the same height as said transfer gate and adjacent to said transfer gate over the whole height;

a first interlayer insulating film having a surface which defines the same surface as the surface of said transfer gate and the surface of said contact plug;

a second interlayer insulating film formed on said first interlayer insulating film; and

diameter-reduced contact plugs which are smaller than said contact plugs and extend through said second interlayer insulating film to conduct to said contact plugs, respectively.

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2. The semiconductor device according to claim 1, further including a memory cell section having a plurality of memory cells,

said memory cell section including, in addition to said transfer gates, said contact plugs, and said first and second interlayer insulating films,

a bit line formed on said second interlayer insulating film;

a third interlayer insulating film formed on said second interlayer insulating film so as to cover said bit line; and

capacitors formed on said third interlayer insulating film;

said memory cell section further including, as said diameter-reduced contact plugs,

Sub A1

a bit line contact plug which extends through said second interlayer insulating film to bring said contact plugs and said bit line into conduction; and

capacitor contact plugs which extend through said second and third interlayer insulating films to bring said contact plugs and said capacitors into conduction.

Sub C1

3. The semiconductor device according to claim 2, wherein said gate electrode layer has a doped silicon layer containing an impurity and a silicide film for covering the surface of the doped silicon layer,

any of said contact plugs corresponding to said capacitors, said capacitor contact plugs, and lower electrodes of said capacitors is formed of doped silicon containing an impurity,

said contact plug corresponding to the bit line has a doped silicon layer containing an impurity and a silicide film formed only at a portion brought into contact with said bit line contact plug, and

said bit line contact plug has a barrier metal brought into contact with said each contact plug and a metal layer formed on the barrier metal.

4. The semiconductor device according to claim 3, wherein said capacitor includes a capacitor insulating film formed of SiON and an upper electrode comprised of doped silicon containing an impurity.

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5. The semiconductor device according to claim 2, further including a logic circuit section including a plurality of transistors, said logic circuit section including, in addition to said transfer gates, said contact plugs, and said first and second interlayer insulating films,

bit lines formed on said second interlayer insulating film; and

said logic circuit section further including, as said diameter-reduced contact plugs,

bit line contract plugs which extend through said second interlayer insulating film to bring said contact plugs and said bit lines into conduction.

6. The semiconductor device according to claim 5, wherein said logic circuit section has NMOS transistors and PMOS transistors both of which constitute CMOS transistors.

7. The semiconductor device according to claim 6, wherein contact plugs and gate electrode layers provided in association with said NMOS transistors respectively have a doped silicon layer containing an N-type impurity, and

contact plugs and gate electrode layers provided in association with said PMOS transistors respectively have a doped silicon layer containing a P-type impurity.

8. The semiconductor device according to claim 6, wherein said memory cell section has transistors each having a first-conduction type,

one of the NMOS transistors and the PMOS transistors having a conduction type different from the first conduction type has a buried channel prepared for the first conduction type semiconductor, and a counter channel formed in a surface region of the buried channel by a semiconductor prepared for a second conduction type,

said each contact plug provided in association with the NMOS transistor has a doped silicon layer containing an N-type impurity,

said each contact plug provided in association with the PMOS transistor has a doped silicon layer containing a P-type impurity, and

any of said gate electrode layers provided in association with the NMOS transistors and said gate electrode layers provided in association with the PMOS transistors has a doped silicon layer containing a first conduction type impurity.

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9. The semiconductor device according to claim 1, further including a logic circuit section including a plurality of transistors, said logic circuit section including, in addition to said transfer gates, said contact plugs, and said first and second interlayer insulating films,

bit lines formed on said second interlayer insulating film; and

said logic circuit section further including, as said diameter-reduced contact plugs,

bit line contact plugs which extend through said second interlayer insulating film to bring said contact plugs and said bit lines into conduction.

10. The semiconductor device according to claim 9, wherein said logic circuit section has NMOS transistors and PMOS transistors both of which constitute CMOS transistors.

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11. The semiconductor device according to claim 10, wherein contact plugs and gate electrode layers provided in association with said NMOS transistors respectively have a doped silicon layer containing an N-type impurity, and

contact plugs and gate electrode layers provided in association with said PMOS transistors respectively have a doped silicon layer containing a P-type impurity.

12. The semiconductor device according to claim 1, wherein said contact plugs and said gate electrode layers respectively have a doped silicon layer containing an impurity and a silicide film for covering the surface of the doped silicon layer, and

said each diameter-reduced contact plug has a barrier metal brought into contact with the silicide film, and a metal layer formed on the barrier metal.

13. The semiconductor device according to claim 1, wherein the gate electrode layer of said transfer gate has a metal layer and a barrier metal which surrounds the metal layer.

14. The semiconductor device according to claim 1, wherein a gate oxide film of said transfer gate is a CVD insulating film formed by a CVD method.

15. The semiconductor device according to claim 1, wherein the gate insulating film of said transfer gate is a thermal oxide film formed by a thermal oxidation method or a thermally-oxidized nitride film formed by a thermal oxidation nitriding method.

16. A method of manufacturing a semiconductor device having contact plugs adjacent to transfer gates, comprising the following steps for:

depositing a first interlayer insulating film on a silicon substrate;

forming transfer gate holding trenches in the first interlayer insulating film;

forming side walls of said each transfer gate in the transfer gate holding trenches;

forming a gate insulating film and a gate electrode layer of said each transfer gate within a space interposed between the side walls;

etching portions adjacent to said transfer gates, of the first interlayer insulating film under a condition that said first interlayer insulating film is capable of being removed at a high selectivity with respect to a material which constitutes said each transfer gate, to thereby form contact holes adjacent to said transfer gates in a self-aligned manner;

forming contact plugs in said contact holes respectively;

forming a second interlayer insulating film on the first interlayer insulating film, the contact plugs and the transfer gates;

forming diameter-reduced contact holes which are smaller than the contact plugs and in communication with the contact plugs, in the second interlayer insulating film; and

forming diameter-reduced contact plugs which conduct to said contact plugs, in the diameter-reduced contact holes.

17. The method according to claim 16, wherein said step for forming the contact holes includes a step for etching the first interlayer insulating film by using a mask pattern having an opening which extends over at least two contact holes.

18. The method according to claim 16, wherein said semiconductor device has a memory cell section having a plurality of memory cells, and further including the steps for:

forming a bit line on a second interlayer insulating film in the memory cell section;

forming a third interlayer insulating film on the second interlayer insulating film so as to cover the bit line; and

forming capacitors on the third interlayer insulating film in the memory cell section; and

wherein said step for forming the diameter-reduced contact plugs includes the sup-steps for:

forming bit line contact plugs in the memory cell section, which extend through the second interlayer insulating film so as to bring the contact plugs and the bit line into conduction, and

forming capacitor contact plugs in the memory cell section, which extend through the second and third interlayer insulating films so as to bring the contact plugs and the capacitors into conduction.

19. The method according to claim 18, wherein said semiconductor device includes a logic circuit section having a plurality of memory cells, and further including the steps for:

forming bit lines on a second interlayer insulating film in the logic circuit section; and

forming a third interlayer insulating film on the second interlayer insulating film so as to cover the bit lines; and

wherein said step for forming said diameter-reduced contact plugs includes a sub-step for forming bit line contact plugs in the logic circuit section, which extend through the second interlayer insulating film so as to bring the contact plugs and the bit lines into conduction.

20. The method according to claim 16, wherein said semiconductor device includes a logic circuit section having a plurality of memory cells, and further including the steps for:

forming bit lines on a second interlayer insulating film in the logic circuit section; and

forming a third interlayer insulating film on the second interlayer insulating film so as to cover the bit lines; and

wherein said step for forming said diameter-reduced contact plugs includes a sub-step for forming bit line contact plugs in the logic circuit section, which extend through the second

interlayer insulating film so as to bring the contact plugs and the bit lines into conduction.